PAGES 2, 8 - 10, 17, 25, 26, 28 - 31, 43, 47, 49, 50, 56, 57, 59 - 61, 63, 64, 66, and 70,

WITH ANNOTATIONS

TO INDICATE REVISIONS, OF U.S. PATENT APPLICATION 09/903,059

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CA and CB. The VCO's oscillator signal, taken from the drain of FET QA or QB, is provided at variable oscillator frequency f_O given as:

$$f_O = \frac{1}{2\pi\sqrt{L_O C_O}} \quad (1)$$

where L_O is the fixed inductance of each of inductors LA and LB, and C_O is the variable alternating-current ("AC") capacitance of each of varactors CA and CB. A control voltage (not shown) is applied to varactors CA and CB to control the value of capacitance C_O and thus oscillator frequency f_O.

[0005] Fig. 2a depicts a conventional single-ended Colpitts VCO formed with n-channel enhancement-mode insulated-gate FET QC, fixed-value inductor LC, current source IC, fixed-value capacitor CC, and varactor CE. A differential version of the single-ended VCO of Fig. 2a is depicted in Fig. 2b. The VCO in Fig. 2b consists of identical common-gate n-channel insulated-gate FETs QC and QD, identical fixed-value inductors LC and LD, identical fixed-value capacitors CC and CD, and varactor CF. Letting L_O here represent the inductance of each of inductors LC and LD, the oscillator in each of Figs. 2a and 2b provides an oscillator signal at variable frequency f_O determined from Eq. 1 where capacitance C_O is now the series combination of (a) the fixed capacitance of each of capacitors CC and CD and (b) either the variable capacitance of varactor CE or twice the variable capacitance of varactor CF. A control voltage (not shown) is applied to varactor CE or CF to control its AC capacitance and thus frequency f_O.

[0006] Varactors such as varactors CA, CB, CE, and CF can be implemented in various ways. A common varactor is a semiconductor junction varactor formed with a p-n diode having a reverse-biased p-n junction. A simplified example of a conventional junction varactor is shown in Fig. 3 where item 20 is a p-type body region of a semiconductor body. Moderately doped (p) material of body region 20 forms p-n junction 22 with heavily doped n-type region 24. Regions 20 and 24 respectively constitute the diode's anode and cathode.

[0007] Cathode electrode 26 contacts cathode region 24 along the upper semiconductor surface. Body electrode 28 contacts body region 20, typically through heavily doped p-type material (not

between body electrode 46 and each junction electrode 56 to reverse bias corresponding p-n junction 54. Since each junction region 52 is of n-type conductivity, each junction electrode 56 is at a higher voltage than body electrode 46. A junction depletion region 58, which normally meets surface depletion region 48, extends along each p-n junction 54.

[0020] Fig. 6 illustrates the situation in which two junction regions 52 are present in a deep depletion insulated-gate varactor. With the two regions 52 being laterally separated from each other, the structure is similar to an insulated-gate FET except that regions 52 are electrically tied together rather than serving as source and drain. When only one region 52 is present, the other region 52 is typically replaced with dielectric material that laterally electrically isolates islands of the semiconductor material along the upper semiconductor surface.

[0021] The deep depletion insulated-gate varactor of Fig. 6 operates in basically the same way as the depletion insulated-gate varactor of Fig. 4 except that the presence of junction region(s) 52 causes inversion layer 50 to occur at a greater positive value of gate-to-body voltage V_{GB} than in an otherwise corresponding depletion varactor. Maximum surface depletion thickness t_{dsmax} in the deep depletion varactor is thus greater than in the corresponding depletion varactor. Referring to curve C of Fig. 5, capacitance ratio C_{VA}/C_{GDA} reaches a lower value with the deep depletion varactor than with the depletion varactor. Accordingly, minimum varactor capacitance value C_{VAmin} reaches a lower value in the deep depletion varactor than in the depletion varactor. As a result, the deep depletion varactor achieves a higher maximum-to-minimum varactor capacitance ratio than the depletion varactor. In particular, the maximum-to-minimum capacitance ratio for a deep depletion varactor can readily be 15 - 20 at state-of-the-art values for gate dielectric thickness t_{GD}.

[0022] Wong et al ("Wong"), "A Wide Tuning Range Gated Varactor," IEEE J. Solid-State Circs., May 2000, pages 773 - 779, describes another type of semiconductor varactor. As generally shown in Fig. 7, Wong's varactor is created from ~~n+~~ n body region 60 of a semiconductor body. Using somewhat unusual terminology, Wong's varactor includes heavily doped ~~n-type~~ p-type "source" 62 and heavily doped ~~p-type~~ n-type "drain" 64 laterally separated from each other along the upper semiconductor surface. Gate dielectric layer 66 separates gate electrode 68 from moderately doped n-type body material situated between source 62 and drain 64. Wong reports that the varactor capacitance is defined as the capacitance looking into the drain node.

[0023] Wong's varactor is operated in two modes with source voltage V_S being ground reference (0 volt) in both modes. In one mode, drain voltage V_D is also at ground while gate voltage V_G is variable. Surface depletion region 70 extends along the upper semiconductor surface below gate electrode 68 and meets drain 64. Surface depletion region 70 merges into junction depletion region 72 extending along the p-n junction between body region 60 and source 62. Reducing gate voltage V_G in this mode causes the thickness of composite depletion region 70/72 to increase so that the varactor capacitance decreases. In the second mode, gate voltage V_G is at ground while drain voltage V_D is variable. Increasing drain voltage V_D causes the thickness of junction depletion region 72 to increase, thereby reducing the varactor capacitance. Inversion along the upper semiconductor surface below gate electrode 68 limits the maximum thickness of junction depletion region 72 and thus the minimum varactor capacitance in this mode.

[0024] Wong reports maximum and minimum capacitance values which appear to yield a maximum-to-minimum varactor capacitance ratio of 3 - 4. This varactor capacitance ratio is relatively low and, in fact, is lower than that typically achievable with either of the depletion insulated-gate varactors described above. As in the other varactors described above, the maximum-to-minimum capacitance ratio in Wong is determined primarily by the device metallurgical structure and is largely not independently controllable by the circuit designer.

[0025] Switched-capacitor varactors are employed in some applications. Although a high maximum-to-minimum varactor capacitance ratio can be achieved with a switched-capacitor varactor, it typically occupies a large semiconductor layout area. Switched-capacitor varactors require switching control and thus are also relatively complex.

[0026] It would be desirable to have a varactor which is of relatively simple design and which can readily achieve a high maximum-to-minimum varactor capacitance ratio. It would also be desirable to be able to change the maximum-to-minimum varactor capacitance ratio by appropriately adjusting certain lateral varactor layout dimensions.

GENERAL DISCLOSURE OF THE INVENTION

[0027] The present invention furnishes a semiconductor junction varactor that employs gate enhancement for enabling the varactor to achieve a high ratio of maximum varactor capacitance to minimum varactor capacitance. The maximum-to-minimum capacitance ratio for the present

gate-enhanced junction varactor can easily be well in excess of 10. More particularly, the present varactor can readily achieve a maximum-to-minimum ~~varactor~~ capacitance ratio in the vicinity of 20 or more. The varactor of the invention is of relatively simple design. No special processing techniques are needed to fabricate the present varactor. Consequently, it can be fabricated according to a semiconductor manufacturing process having a capability for providing p-n diodes and insulated-gate FETs.

[0028] Importantly, the maximum-to-minimum capacitance ratio for the gate-enhanced junction varactor of the invention depends on the amount of gate enhancement, a feature determined by the varactor's lateral dimensions. Accordingly, the maximum-to-minimum capacitance ratio can be set to achieve a specific value by appropriately selecting the varactor's lateral dimensions. The present varactor can thereby be readily incorporated into a general methodology for laying out and fabricating integrated circuits. In addition, the lateral area occupied by the varactor of the invention is small compared to that occupied by an otherwise comparable switched-capacitor varactor.

[0029] More particularly, a varactor configured according to the invention contains a plate region and a body region of a semiconductor body. The plate and body regions are of opposite conductivity type and meet each other to form a p-n junction. A dielectric layer is situated over the semiconductor body and contacts the body region. A gate electrode is situated over the dielectric layer at least where the dielectric layer contacts material of the body region. Plate and body electrodes are respectively connected to the plate and body regions.

[0030] The capacitance of the present gate-enhanced junction varactor is taken between the plate and body electrodes. A suitable plate-to-body bias voltage of a variable magnitude is applied between the plate and body electrodes so that the p-n junction is not conductively forward biased. The p-n junction is normally reversed biased over the large majority of the range across which the plate-to-body voltage varies. A junction depletion region extends along the p-n junction. With a suitable gate-to-body bias voltage applied between the gate and body electrodes, a surface depletion region is formed in the body region below the gate electrode and merges with the junction depletion region. The gate-to-body voltage is controlled in such a way that an inversion layer forms in the surface depletion region at a certain value of the plate-to-body voltage. The inversion layer disappears when the plate-to-body voltage is appropriately adjusted in a specified (positive or negative) manner.

where plate voltage V_P and body voltage V_B are defined relative to an arbitrary reference point such as ground potential (again, 0 V).

[0070] The structure of Fig. 8 functions as a varactor in accordance with the invention when p-n junction 104 is not forward biased so as to conduct significantly. Accordingly, the magnitude and polarity of plate-to-body voltage V_R are controlled such that junction 104 is either reversed biased or is forward biased but below the threshold point for significant conduction. When junction 104 is reverse biased, plate voltage V_P is at a higher DC electrical potential than body voltage V_B since plate region 102 is of n-type conductivity. Plate-to-body voltage V_R is then positive.

[0071] When p-n junction 104 is forward biased below the threshold conductive point, plate-to-body voltage V_R is negative but exceeds a negative junction threshold value V_{R0} at which junction 104 first becomes significantly forwardly conductive. Negative junction threshold value V_{R0} generally equals $-V_F$ where V_F is the forward voltage drop of 0.6 - 0.7 V at which a p-n junction, i.e., junction 104 here, becomes significantly conductive in the forward direction. Hence, junction threshold value V_{R0} is normally -0.6 - -0.7 V, typically -0.7 V. Overall, voltage V_R is controlled so as to be greater than negative junction threshold value V_{R0}.

[0072] With body voltage V_B applied to body electrode 116, gate-to-body bias voltage V_{GB} is applied between gate electrode 112 and body electrode 116 by applying a DC gate voltage V_G to gate electrode 112. Gate-to-body voltage V_{GB} is specifically defined as:

$$V_{GB} = V_G - V_B \tag{11}$$

where gate voltage V_G is defined relative to the same arbitrary reference point, e.g., ground, as plate voltage V_P and body voltage V_B. Gate-to-body voltage V_{GB} is generally at least zero and is normally positive. As discussed further below, voltage V_{GB} is normally substantially constant or is controlled as a function of plate-to-body voltage V_R.

[0073] Under the preceding conditions for bias voltages V_R and V_{GB}, a junction depletion region 118 extends along p-n junction 104. Junction depletion region 118 consists of a body-side

$$C_{VAmin} = \frac{K_{SC}\varepsilon_0 A_P}{(A_P + A_I)t_{dJmax}} \tag{21}$$

where t_{dJmax} is the maximum value of thickness t_{dJ} of junction depletion region 118 when voltage V_R equals V_{Rmax}.

[0095] By combining Eqs. 14 and 21, the ratio of maximum varactor areal capacitance C_{VAmax} to minimum varactor areal capacitance C_{VAmin} for the varactor of Fig. 8 is approximately:

$$\frac{C_{VAmax}}{C_{VAmin}} = \left(\frac{t_{dJmax}}{t_{dJmin}}\right) + \left(\frac{A_I}{A_P}\right)\left(\frac{t_{dJmax}}{t_{dsmin}}\right) \tag{22}$$

Per the approximation of Eq. 22, the maximum-to-minimum varactor capacitance ratio for the present gate-enhanced junction varactor is a function of (a) the maximum-to-minimum thickness ratio t_{dJmax}/t_{dJmin} for junction depletion region 118, (b) the gate-enhancement area ratio A_I/A_P of inversion area A_I to plate area A_P, and (c) the mixed gate-enhancement thickness ratio t_{dJmax}/t_{dsmin} of maximum junction depletion thickness t_{dJmax} to minimum surface depletion thickness t_{dsmin}.

[0096] Thickness values t_{dJmax} and t_{dJmin} for junction depletion region 118 can be determined approximately from Eq. 3 presented above for the conventional junction varactor of Fig. 3. For uniform acceptor body dopant concentration N_B in region 118, the maximum-to-minimum thickness ratio for region 118 is approximately:

$$\frac{t_{dJmax}}{t_{dJmin}} = \sqrt{\frac{V_{Rmax} + V_{BI}}{V_{Rmin} + V_{BI}}} \tag{23}$$

where V_{BI} is the built-in voltage of p-n junction 104. The right-hand side of Eq. 23 is the maximum-to-minimum varactor capacitance ratio given by Eq. 4 for the conventional junction varactor of Fig. 3 at uniform body dopant concentration in body-side portion 32 of junction depletion region 30. If gate electrode 110 were absent so that inversion area A_I is zero in the varactor of Fig. 8, the capacitance ratio given by Eq. 22 for the present gate-enhanced junction varactor would (as expected) devolve to that given by Eq. 4 for the conventional junction varactor.

[0097] In addition to the t_{dJmax}/t_{dJmin} junction depletion thickness ratio, the maximum-to-minimum varactor capacitance ratio for the varactor of Fig. 8 contains, as indicated by Eq. 22, a factor $\frac{(A_I/A_P)(t_{dJmax}/t_{dsmin})}{(A_I/A_P)(t_{dJmax}/t_{dJmin})}$ that arises from the gate enhancement. The t_{dJmax}/t_{dsmin} mixed gate-enhancement thickness ratio is greater than 1. Accordingly, the maximum-to-minimum varactor capacitance ratio for the varactor of Fig. 8 can be made quite high by choosing the A_I/A_P gate-enhancement area ratio to be high.

[0098] For example, minimum surface depletion thickness t_{dsmin} typically approximately equals minimum junction depletion thickness t_{dJmin}. Typical values for end-point voltages V_{Rmax} and V_{Rmin} are 2 and -0.5 V. With built-in voltage V_{BI} being approximately 0.9 V, application of Eq. 23 yields a value of 2.5 - 3 for each of thickness ratios t_{dJmax}/t_{djmin} and t_{dJmax}/t_{dsmin}. At a moderate A_I/A_P area ratio of 4, the C_{VAmax}/C_{VAmin} capacitance ratio is 10 - 15 for the varactor of Fig. 8. For a higher A_I/A_P area ratio of 8 - 10, the C_{VAmax}/C_{VAmin} ratio is 20 - 30. The varactor of Fig. 8 can achieve yet higher values of the maximum-to-minimum capacitance ratio by utilizing values of the A_I/A_P area ratio in excess of 10.

[0100] Fig. 9a illustrates a silicon-gate implementation of the n-channel gate-enhanced junction varactor of Fig. 8 in accordance with the invention. In the implementation of Fig. 9a, body electrode 116 contacts body region 100 along upper semiconductor surface 106 through a heavily doped p-type body contact portion 132 of region 100. Body contact portion 132 is spaced laterally apart from surface depletion region 126 and also from junction depletion region 118.

[0101] Gate electrode 112 here consists of very heavily doped n-type polysilicon. Hence, gate electrode 112 is of the same conductivity type (n-type) as plate region 102. Two portions of electrode 112 are depicted in Fig. 9a. These two portions can be two laterally separated gate

[0105] Gate electrode 112 in the implementation of Fig. 9b consists of a lower electrode portion 112L and an upper electrode portion 112U. Lower electrode portion 112L is formed with very heavily doped n-type polysilicon. Similar to what occurs in the implementation of Fig. 9a, lower electrode portion 112L is thus of the same conductivity as plate region 102. Upper electrode portion 112U consists of metal or/and metal silicide. Similar to what was said above about gate electrode 112 in Fig. 9a, the two portions of electrode 112 shown in Fig. 9b can be connected together outside the plane of Fig. 9b to form a single, normally annular, electrode 112. The two illustrated electrode portions can also be two laterally separated gate electrodes 112.

[0106] The gate-enhanced junction varactor of the present invention can be implemented in p-channel versions as well as n-channel versions. Analogous to Fig. 8, Figs. 10a and 10b (collectively "Fig. 10") illustrate a general p-channel gate-enhanced junction varactor in accordance with the invention at two stages of varactor operation. The p-channel junction varactor of Fig. 10 is formed from a semiconductor body containing an n-type body region 150 and a very heavily doped p-type plate region 152 that meets body region 150 to form a p-n junction 154. Items 156 and 158 in Fig. 10 indicate the upper and lower surfaces of the semiconductor body.

[0107] In addition, the p-channel junction varactor of Fig. 10 contains a gate dielectric layer 160, a gate electrode 162, a plate electrode 164, a body electrode 166, a junction depletion region 168 consisting of a body-side portion 170 and a plate-side portion 172, undepleted p-type material 174 of plate region 152, a surface depletion region 176, and undepleted n-type material 178 of body region 150. An inversion layer 180, here consisting of holes, is formed along upper semiconductor surface 156 below gate dielectric layer 160 and gate electrode 162 to meet ~~p-n junction~~ plate region 152. Voltages V_G, V_P, and V_B are respectively applied to electrodes 162, 164, and 166 in the p-channel varactor of Fig. 10 to establish gate-to-body voltage V_{GB} and plate-to-body voltage V_B according to Eqs. 10 and 11 just as voltages V_G, V_P, and V_B are applied to electrodes ~~142, 144, and 146~~ 112, 114, 116 in the n-channel varactor of Fig. 8.

[0108] Components 150, 152, 154, 160, 162, 166, 168, 170, 172, 174, 176, and 178 in the p-channel varactor of Fig. 10 are respectively configured the same as components 100, 102, 104, 110, 112, 114, 116, 118, 120, 122, 124, 126, and 128 in the n-channel varactor of Fig. 8. Likewise, inversion layer 180 forms at the same relative location in the varactor of Fig. 10 as does inversion layer 130 in the varactor of Fig. 8. The operational stages of Figs. 10a and 10b

respectively correspond to the operational stages of Figs. 8a and 8b. Subject to the voltage polarities being respectively reversed in the varactor of Fig. 10 compared to the varactor of Fig. 8 and subject to the voltage changes occurring respectively in the opposite directions in the varactor of Fig. 10 than in the varactor of Fig. 8, the p-channel varactor of Fig. 10 functions in the same way, benefits from gate enhancement in the same way, and is employed in the same way as the n-channel varactor of Fig. 8. Eqs. 12 - 23 thus apply directly to the p-channel varactor of Fig. 10.

[0109] Figs. 11a and 11b illustrate electronic symbols suitable for respectively representing the n-channel and p-channel gate-enhanced junction varactors of the invention. The plus and minus signs in Figs. 11a and 11b indicate the voltage polarities utilized during all, or nearly all, of the operation of the present n-channel and p-channel junction varactors.

Transition Voltage

[0110] Transition voltage V_X, the value of plate-to-body bias voltage V_R at which inversion layer 130 or 180 disappears, is derived in the following manner as a function of gate-to-body voltage V_{GB}. The derivation of transition voltage V_X is performed under the general simplifying assumptions employed in Grove, Physics and Technology of Semiconductor Devices (John Wiley & Sons), 1967, and does not include quantum-mechanical threshold-voltage corrections typically associated with values of gate dielectric thickness t_{GD} less than 10 nm. The derivation is done here for the n-channel varactor of Fig. 8 but, with appropriate reversals in voltage polarities, applies to the p-channel varactor of Fig. 10.

[0111] The V_X derivation is done for a stripe-type (rectangular) geometry rather than an annular or other three-dimensional geometry. That is, device characteristics are assumed to vary in two directions (or dimensions), namely, the vertical direction and one of the remaining two orthogonal directions, but not in the other of the remaining two orthogonal directions. The results of the derivation are qualitatively applicable to an annular geometry and are quantitatively applicable to an annular geometry for situations in which the radii of curvature in the annular geometry are much greater than the gate-dielectric and depletion-region thicknesses involved in the electric-field determinations.

[0112] Assume that acceptor dopant concentration N_B in the body material that forms surface depletion region 126 and body-side portion 120 of junction depletion region 118 in the varactor

of Fig. 8 is uniform. For simplicity, also assume that body voltage V_B is ground reference (0 V). The V_X derivation can then be done in terms of plate-to-body voltage V_R and gate-to-body voltage V_{GB} without reference to plate voltage V_P and gate voltage V_G since they respectively equal voltages V_R and V_{GB} when body voltage V_B is ground.

[0113] Consider the situation in which plate-to-body voltage V_R is initially zero. Further assume that gate-to-body bias voltage V_{GB} is at a fixed positive value, i.e., initial value V_{GBi}, greater than gate threshold value V_{T0} where V_{T0} is again the value of voltage V_{GB} at which inversion onsets when voltage V_R is zero. Since voltage V_{GB} is greater than threshold value V_{T0}, inversion layer 130 is present. The varactor of Fig. 8 is in a condition of strong inversion.

[0114] Let V_{IL} generally represent the DC electrical potential of inversion layer 130 in Fig. 8. Neglecting the vertical potential drop in layer 130, inversion-layer potential V_{IL} is at an initial DC value V_{ILi} given as follows when plate-to-body voltage V_R is zero and the varactor of Fig. 8 is in strong inversion:

$$\begin{aligned} V_{ILi} &= \Phi_{s,inv} \\ &= 2\Phi_{Fp} \end{aligned} \tag{24}$$

where $\Phi_{s,inv}$ is the surface potential at inversion, and Φ_{Fp} is the Fermi potential of the p-type semiconductor material in surface depletion region 126. Fermi potential Φ_{Fp} is determined from:

$$\Phi_{Fp} = \left(\frac{kT}{q}\right)\ln\left(\frac{N_B}{n_i}\right) \tag{25}$$

where k is Boltzmann's constant, T is the temperature, and n_i is the intrinsic carrier concentration.

[0115] Let V_{PR} represent the DC electrical potential of plate region 102 in Fig. 8. Even though plate-to-body potential V_R is zero, plate-region potential V_{PR} is at an initial positive DC value V_{PRi} due to built-in potential V_{BI} across p-n junction 104. Initial value V_{PRi} is given as:

$$\begin{aligned} V_{PRi} &= \Phi_{Fp} + \Phi_{Fn} \\ &\approx 2\Phi_{Fp} \end{aligned} \tag{26}$$

where V_{Fn} is the Fermi potential of the n-type semiconductor material in plate region 102. Since plate-region potential V_{PR} approximately equals inversion-layer potential V_{IL} at this point, the electrons in inversion layer 130 have no physical impetus for leaving layer 130 and thus stay in layer 130 close to upper semiconductor surface 106.

[0116] Gate dielectric layer 112 takes up the potential between body region 100 and inversion layer 130. The DC potential difference V_{GD} across gate dielectric 112 is at an initial DC value V_{GDi} given as:

$$\begin{aligned} V_{GDi} &= V_{GB} - V_{FB} - V_{ILi} \\ &\approx V_{GB} - V_{FB} - 2\Phi_{Fp} \end{aligned} \tag{27}$$

where V_{FB} is the flat-band voltage.

[0117] The electronic charge in inversion layer 130 and surface depletion region 126 consists of surface electrons in layer 130 and bulk ionized acceptor atoms in region 126 and layer 130. Let Q_{nA} represent the charge per unit area of the electrons in inversion layer 130 while Q_{BA} is the charge per unit area of ionized acceptor atoms in depletion region 126 and layer 130. Areal charges Q_{nA} and Q_{BA} are both negative in sign and have respective initial values Q_{nAi} and Q_{BAi} when gate-to-body voltage V_B is at initial value V_{GBi} while plate-to-body voltage V_R is zero.

may, in some cases, be of substantially zero impedance (0 ohm). Hence, component ZH or ZL can be simply an electrical line.

[0150] High-bias impedance component ZH is part of a high-bias electrically conductive DC path which extends through circuit 230 and through which high-bias capacitance signal path line 236 is electrically coupled to the V_{HH} high voltage supply. Low-bias impedance component ZL is similarly part of a low-bias electrically conductive DC path which extends through circuit 230 and through which low-bias capacitance signal path line 238 is electrically coupled to the V_{LL} low voltage supply.

[0151] Varactor control system 232 furnishes varactor C1 with gate voltage V_G and body voltage V_B at values which normally vary during circuitry operation but whose difference V_{GB} is maintained largely constant at initial value V_{GBi}. In particular, gate electrode 112 of varactor C1 receives gate voltage V_G on a high-bias control line 240 connected to control system 232. Body electrode 116 similarly receives voltage V_B on a low-bias control line 242 connected to system 232. Since varactor C1 is of n-channel type, voltage V_G on high-bias control line 240 is normally greater than voltage V_B on low-bias control line 242.

[0152] Control system 232 contains a high-bias DC voltage source 244 and a low-bias DC voltage source 246. High-bias voltage source 244 is coupled between high-bias control line 240 and low-bias path line 238 by way of an electrical line 248. Low-bias voltage source 246 is similarly coupled between low-bias control line 242 and path line 238 by way of an electrical line 250. Voltage sources 244 and 246 thus respectively furnish DC gate voltage V_G and DC body voltage V_B.

[0153] Low-bias voltage source 246 is in the capacitance signal path since body electrode 116 is in the capacitance signal path. Accordingly, the capacitance signal path consists of high-bias path line 236, plate electrode 114, body electrode 116, low-bias control line 242, low-bias voltage source 246, electrical line 250, and low-bias path line 238. Gate electrode 112 is outside the capacitance signal path. Also, control system 232 is normally connected between the V_{HH} and V_{LL} voltage supplies.

[0154] Gate-to-body voltage V_{GB} is, as indicated above, provided at largely constant value V_{GBi} to varactor C1 during operation of the electronic circuitry in Fig. 17. Since voltage sources 244 and 246 respectively provide gate voltage V_G and body voltage V_B whose difference is

[0167] In some implementations of the circuitry of Fig. 17, DC plate voltage V_P can vary during circuitry operation provided that voltage V_P varies differently than body voltage V_B. The variation in voltage V_P is achieved by appropriately varying internal voltage drop V_K. Body voltage V_B can, in fact, sometimes be largely constant (relative to low supply voltage V_{LL}). In any event, DC plate-to-body voltage V_R varies upward or downward to adjust the C_V value as needed.

[0168] The general circuitry of Fig. 17 can be readily modified to use a p-channel version of the present gate-enhanced junction varactor in place of n-channel junction varactor C1. One way of implementing this modification is to reconfigure the circuitry so that it is interconnected in a complementary (mirror-image) manner to what is shown in Fig. 17. That is, high-bias capacitance signal path line 236 can be connected directly to voltage sources 244 and 246 in control system 232. Using the electrode reference symbols of Fig. 10, low-bias capacitance signal path line 238 is connected to plate electrode 164 of the p-channel varactor. With the polarity direction of voltage sources 244 and 246 reversed, ~~plate~~ gate electrode 162 and body electrode 166 of the p-channel varactor are respectively connected to voltage sources 244 and 246. Due to the polarity direction reversal, voltage source 244 provides gate voltage V_G at a lower value than body voltage V_B provided by voltage source 246. When present, level shifter 234 is connected between circuit 230 and the V_{LL} supply.

[0169] An extension, or application, in accordance with the invention of the general electronic circuitry of Fig. 17 to the use of a pair of n-channel versions of the present varactor with symmetrical circuitry is presented in Fig. 18. As in the circuitry of Fig. 17, gate-to-body voltage V_{GB} is maintained approximately constant during varactor operation in the general electronic circuitry of Fig. 18. The components of the electronic circuitry of Fig. 18 consist of a general symmetrical electronic circuit 260, a pair of largely identical n-channel gate-enhanced junction varactors C1 and C2 configured according to the invention, varactor control system 232, and optional level shifter 234.

[0170] The electronic circuitry, primarily symmetrical circuit 260, in Fig. 18 has a pair of capacitance signal paths for respectively receiving varactors C1 and C2 in order to enable the circuitry to perform an electronic function dependent on variable capacitances C_V of varactors C1 and C2. Plate electrodes 114 and body electrodes 116 of capacitors C1 and C2 are situated in the capacitance signal paths. Analogous to the electronic circuitry of Fig. 17, one end of the C1

[0174] Internal circuitry 260I is also connected to the V_{LL} low voltage supply. To the extent that circuitry 260I is connected by multiple paths to the V_{LL} supply, these connections are made in a symmetrical manner relative to high-bias impedance components Z1 and Z2. Although not indicated in Fig. 18, circuitry 260I may be coupled to the V_{HH} high voltage supply by multiple symmetrical paths separate from those that go through components Z1 and Z2. As a result, circuit 260 is internally symmetrical and is symmetrically arranged with respect to varactors C1 and C2.

[0175] Varactor control system 232 in the circuitry of Fig. 18 is configured with respect to, and controls, varactor C1 in the same manner as in the circuitry of Fig. 17. Control system 232 in the circuitry of Fig. 18 is also configured with respect to, and controls, varactor C2 the same as varactor C1. Hence, system 232 furnishes each of varactors C1 and C2 with gate voltage V_G and body voltage V_B at values which normally vary during circuitry operation but whose difference V_{GB} is held largely constant at initial value V_{GBi}. In particular, high-bias DC voltage source 244 provides gate voltage V_G on high-bias control line 240 to gate electrode 112 of each of varactors C1 and C2. Low-bias voltage source 246 provides body voltage V_B on low-bias control line ~~248~~ 242 to body electrode 116 of each of varactors C1 and C2.

[0176] Neither low-bias capacitance signal path line 236 nor one or more low-bias impedance components analogous to low-bias impedance ZL in the circuitry of Fig. 17 appears in the circuitry of Fig. 18. Rather than being connected through electrical lines 248 and 250 to low-bias path line 238, voltage sources 244 and 246 in control system 232 are connected by electrical lines 248 and 250 directly to the V_{LL} low voltage supply in the circuitry of Fig. 18.

[0177] The second (other) ends of the C1 and C2 capacitance signal paths terminate at the V_{LL} low voltage supply in the circuitry of Fig. 18. With low-bias control line 242 connected to body electrodes 116 of both of varactors C1 and C2, the C1 capacitance signal path here consists of high-bias path line 236, C1 plate electrode 114, C1 body electrode 116, low-bias control line 242, low-bias voltage source 246, and electrical line 250. The C2 capacitance signal path signal path similarly consists of further high-bias path line 262, C2 plate electrode 114, C2 body electrode 116, line 242, voltage source 246, and line 250. Gate electrodes 112 of varactors C1 and C2 are outside the capacitance signal paths.

[0178] Alternatively, varactors C1 and C2 may be considered to be in a single capacitance signal path that bypasses low-bias voltage source 246. In that case, the single capacitance signal path in the circuitry of Fig. 18 consists of high-bias path line 236, C1 plate electrode 114, C1 body electrode 116, low-bias control line 242, C2 body electrode 116, C2 plate electrode 114, and further high-bias path line 262. Gate electrodes 112 are outside the single capacitance signal path. Due to (a) the symmetrical arrangement of varactors C1 and C2 relative to symmetrical circuit 260 and (b) the common symmetrical way in which control system 232 controls varactors C1 and C2, the values of capacitances C_V of varactors C1 and C2 are substantially the same at any time during circuitry operation. Since varactors C1 and C2 are in series with each other, the varactor capacitance in the single capacitance signal path is $C_V/2$, i.e., the series combination of two capacitances C_V.

[0179] Level shifter 234 is present in some implementations of the circuitry of Fig. 18 but not in others. Analogous to the positioning of shifter 234 in the circuitry of Fig. 17, shifter 234 here is connected between electronic circuit 260 and the V_{HH} high voltage supply. In particular, shifter 234 is connected to each of the Z1 and Z2 high-bias DC paths so as to be electrically coupled to each of high-bias path lines 236 and 262. When shifter 232 is present, circuit 260 effectively receives, by way of the Z1 and Z1 high-bias DC paths, a high supply voltage which is shifter DC voltage drop V_{LS} lower than high supply voltage V_{HH} provided to control system 232. In the absence of shifter 232, circuit 260 receives the same high supply voltage, i.e., V_{HH}, as system 232.

[0180] Subject to the above-mentioned configurational differences, the circuitry of Fig. 18 operates similarly to, but in a symmetrical manner compared to, the circuitry of Fig. 17. Plate voltages V_P and V_{PF}, the DC portions of respective composite plate voltages v_P and v_{PF} provided from circuit 260 to plate electrodes 114 of varactors C1 and C2 are maintained largely constant. Each DC plate voltage V_P or V_{PF} exceeds body voltage V_B. Due to the circuitry symmetry, plate voltages V_P and V_{PF} are largely equal.

[0181] Composite plate-to-body voltage v_R consisting of DC plate-to-body bias voltage V_R and AC plate-to-body voltage v_r is applied between electrodes 114 and 116 of varactor C1 in the circuitry of Fig. 18 just as in the circuitry of Fig. 17. With low-bias control line 242 also providing body voltage V_B to body electrode 116 of varactor C2, a further composite plate-to-body bias voltage v_{RF} consisting of a further DC plate-to-body bias voltage V_{RF} and a further AC

where constant α is normally less than 1, e.g., 0.79 in the linear approximation of Fig. 12. Rearranging Eq. 43 yields the condition:

$$V_{GB} = \frac{V_R}{\alpha} - V_{T0} \tag{44}$$

for varying voltage V_{GB} so as to avoid the sharp C_{VW} changes depicted in Fig. 16. Adjusting voltage V_{GB} generally in accordance with Eq. 44 results in voltage V_{GB} varying linearly with voltage V_R. Because constant α is normally less than 1, implementing the condition of Eq. 44 can sometimes be difficult.

[0201] A suitable alternative to the condition of Eq. 44 is to control gate-to-body voltage V_{GB} so that it satisfies the relationship:

$$V_{GB} = V_R + V_{GP} \tag{45}$$

where V_{GP} is a non-zero constant voltage value. As with Eq. 44, adjusting voltage V_{GB} in accordance with Eq. 45 results in voltage V_{GB} varying linearly with plate-to-body voltage V_R. Importantly, the condition of Eq. 45 is easier to implement because voltage V_R in Eq. 45 is not multiplied by a non-unitary factor such as constant α in Eq. 44. Imposing the condition of Eq. 45 specifically requires that voltage V_{GB} directly track voltage V_R, or vice versa.

[0202] Voltage difference $V_{GB} - V_R$ is the gate-to-plate voltage for the present varactor. Accordingly, the condition of Eq. 45 requires that the gate-to-plate voltage be held constant at a suitable non-zero value.

[0203] Fig. 20a illustrates how widthwise lineal capacitance C_{VW} varies with plate-to-body voltage V_R for the simulated varactor of Fig. 15 when gate-to-body voltage is adjusted according to the condition of Eq. 45 with gate-to-plate voltage V_{GP} being set at zero-point gate threshold

value V_{T0}, approximately 0.45 V. See curve 266 defined by circles in Fig. 20a. For reference purposes, Fig. 20a also repeats the six curves of Fig. 16 at constant values of voltage V_{GB}. As curve 266 indicates, adjusting voltage V_{GB} so that voltage V_{GP} is held constant at threshold value V_{T0} enables capacitance C_{VW} to decrease gradually with increasing voltage V_R and thereby avoids the sharp C_{VW} change that occur when voltage V_{GB} is constant. This significantly facilitates controlling the varactor capacitance and alleviates problems caused by noise in the control path.

[0204] Fig. 20b depicts how lineal capacitance C_{VW} varies with plate-to-body voltage V_R for the present simulated varactor when gate-to-body voltage V_{GB} is controlled according to Eq. 45 with gate-to-plate voltage V_{GB} fixed at values ranging from 0.3 V in 0.1-V increments to 0.6 V. See curves 268A, 268B, 268C, and 268D defined by circles in Fig. 20b. As in Fig. 20a, the six curves of Fig. 16 at constant values of voltage V_{GB} are also repeated in Fig. 20b for reference purposes.

[0205] Curves 268A, 268B, 268C, and 268D in Fig. 20b show that the C_{VW} variations with plate-to-body voltage V_R becomes progressively more gradual as gate-to-plate voltage V_{GP} is raised from a constant value of 0.3 V to a constant value of 0.6 V. Also, capacitance C_{VW} for each of curves 268A, 268B, 268C, and 268D changes approximately linearly with increasing voltage V_R over the majority of the minimum-to-maximum varactor capacitance range. This further simplifies controlling the varactor capacitance as a function of voltage V_R.

[0206] Among the four values of gate-to-plate voltage V_{GB} presented in Fig. 20b, fixing voltage V_{GP} at 0.6 V as represented by curve 268D generally enables the varactor capacitance to be controlled best because the change in varactor capacitance with increasing plate-to-body voltage V_R is most gradual. Other considerations may place the optimum value of voltage V_{GB} at a point between 0.5 V and 0.6 V.

Further Electronic Circuitry Containing Gate-enhanced Junction Varactor

[0207] Fig. 21 illustrates general electronic circuitry configured in accordance with the invention for utilizing an n-channel version of the present gate-enhanced junction varactor in which gate-to-body bias voltage V_{GB} varies with plate-to-body bias voltage V_R in such a way that gate-to-plate bias voltage V_{GP} is held largely constant at a suitable non-zero value. The electronic circuitry of Fig. 21 is connected between voltage supplies V_{HH} and V_{LL}. The components of the

or/and one or more active electrical elements. Any of components ZH, ZL, ZT, and ZU can be of substantially zero impedance in some implementations of circuit 270. Each component ZH, ZL, ZT, or ZU can thus sometimes simply be an electrical line.

[0212] High-bias impedance component ZH is part of a high-bias DC electrically conductive path which extends through circuit 270 and through which high-bias capacitance signal path line 236 is electrically coupled to voltage setter 274. Analogous to what occurs in the circuitry of Fig. 17, low-bias impedance component ZL here is part of a low-bias electrically conductive DC path which extends through circuit 270 and through which low-bias capacitance signal path line 238 is electrically coupled to the V_{LL} low voltage supply.

[0213] Impedance component ZT is part of an electrically conductive DC path which extends through circuit 270 and through which voltage setter 274 is electrically coupled to the V_{HH} high voltage supply. Since the ZH high-bias DC path electrically couples high-bias path line 236 to setter 274, the ZH and ZT DC paths are parts of a longer electrically conductive DC path through which path line 236 is electrically coupled to the V_{HH} supply. Impedance component ZU is part of an electrically conductive DC path which extends through circuit 270 and through which an electrical line 276 connected to gate electrode 112 of varactor C1 is electrically coupled to the V_{HH} supply.

[0214] Varactor control system 272 furnishes varactor C1 with DC body voltage V_B at a bias value which normally varies during circuitry operation. In particular, gate electrode 112 of varactor C1 receives body voltage V_B on low-bias control line 242 connected to control system 270. Voltage V_B is provided from a low-bias voltage source 278 connected between control line 242 and low-bias capacitance signal path line 238.

[0215] With body electrode 116 of varactor C1 being in the capacitance signal path, voltage source 278 of control system 272 is in the capacitance signal path. Hence, the capacitance signal path here consists of high-bias path line 236, electrodes 114 and 116, control line 242, voltage source 278, and low-bias path line 238. Gate electrode 112 of varactor C1 is again outside the capacitance signal path. Also, control system 272 is normally connected between the V_{HH} and V_{LL} voltage supplies.

[0216] A composite gate voltage v_G consisting of DC ~~plate~~ gate voltage V_G and an AC ~~plate~~ gate voltage v_g is provided from electronic circuit 270 on electrical line 276 to gate electrode 112 of varactor

C1. Impedance component ZU is of such a nature in some implementations of circuit 270 that substantially no DC voltage drop occurs across component ZU. Since the ZU DC path connects line 276 to the V_{HH} high voltage supply, DC gate-plate voltage V_G is then simply high voltage supply V_{HH}, normally substantially constant. In further implementations where component ZU is of substantially zero impedance, AC gate-plate voltage v_g is substantially zero. Composite gate-plate voltage v_G then devolves to DC gate-plate voltage V_G which equals V_{HH}.

[0217] Voltage setter 274 is, as indicated above, connected between the ZT DC path and the ZH high-bias DC path. With the ZT DC path being connected to the V_{HH} high voltage supply, setter 274 receives current from the V_{HH} supply. As this current flows through setter 274 to circuit 270, a largely constant voltage drop V_{VS} occurs across setter 274. The magnitude of voltage drop V_{VS} can be controlled substantially solely by setter 274 or by setter 274 in combination with one or more circuitry elements in circuit 270.

[0218] With DC voltages V_P and V_B again being referenced to low supply voltage V_{LL}, the circuitry of Fig. 21 operates generally in the following manner. Voltage setter 274 and impedance components ZH, ZT, and ZU of circuit 270 together apply a composite gate-to-plate voltage v_{GP} between gate electrode 112 and plate electrode 114 at a suitable non-zero value. Composite gate-to-plate voltage v_{GP} consists of DC gate-to-plate bias voltage V_{GP} and an AC gate-to-plate voltage v_{gp}. Components ZH, ZT, and ZU are normally of such a nature that a largely constant DC voltage drop V_Z occurs across them. This causes gate-to-plate bias voltage V_{GP} to equal the sum of DC impedance voltage drop V_Z and DC setter voltage V_{VS}. Voltage V_{GP} is thus largely constant at a non-zero value during circuitry operation.

[0219] In some implementations of circuit 270, impedance components ZH, ZT, and ZU are of such a nature that DC impedance voltage drop V_Z is very close to zero. Gate-to-plate bias voltage V_{GP} then approximately equals DC setter voltage V_{VS}. Regardless of whether impedance voltage V_Z is zero or some positive constant value, voltage setter 274 controls the value of voltage V_{GP}. Importantly, voltage V_{GP} is controlled by the circuitry of Fig. 21 so as to be largely constant during circuitry operation.

[0220] DC gate voltage V_G is often largely constant at high supply voltage V_{HH} or at a value close to, but less than, V_{HH} in the circuitry of Fig. 21. Voltage V_G largely equals V_{HH} when impedance component ZU is of such a nature that largely no DC voltage drop occurs component

ZU. In any event, the sum of DC plate voltage V_P and DC plate-to-gate voltage V_{GP} equals gate voltage V_G. Since gate-to-plate voltage V_{GP} equals the sum of largely constant voltages V_{VS} and V_Z, plate voltage V_P is a largely constant amount $V_{VS} + V_Z$ below gate voltage V_G. For the exemplary situation in which gate voltage V_G is largely V_{HH} with impedance voltage drop V_Z being largely zero, plate voltage V_P is largely fixed at $V_{HH} - V_{VS}$.

[0221] A composite gate-to-body voltage v_{GB} consisting of DC gate-to-body bias voltage V_{GB} and an AC gate-to-body voltage v_{gb} is applied between electrodes 112 and 116 of varactor C1. Unlike the circuitry of Fig. 17 where AC gate-to-body voltage v_{gb} is zero (or is not present), voltage v_{gb} is present at a variable value in the circuitry of Fig. 21 when impedance component ZU is of non-zero impedance so that AC gate voltage v_g is present at a variable value. As in the circuitry of Fig. 17, composite plate-to-body voltage v_R consisting of DC plate-to-body bias voltage V_R and AC plate-to-body voltage v_r is applied here between electrodes 114 and 116 of varactor C1. DC gate-to-body bias voltage V_{GB} equals DC plate-to-body bias voltage V_R plus gate-to-plate bias voltage V_{GP}. Inasmuch as DC gate-to-plate voltage V_{GP} equals the sum of voltages V_{VS} and V_Z, DC gate-to-body voltage V_{GB} equals the sum of voltages V_R, V_{VS}, and V_Z. Again, impedance voltage V_Z is sometimes zero or close to zero.

[0222] In addition to often being largely constant at high supply voltage V_{HH} or at a value close to V_{HH}, DC gate voltage V_G is normally greater than DC body voltage V_B. Adjusting body voltage V_B upward or downward produces an opposite change in gate-to-body voltage V_{GB} which, in turn, produces an opposite change in plate-to-body voltage V_R while gate-to-plate voltage V_{GP} is being held largely constant at $V_{VS} + V_Z$, often approximately V_{VS}. Varactor C1 again operates internally as described above in connection with ~~Fig. 7~~ the varactor of Fig. 8. Varactor capacitance C_V is thereby adjusted in the way generally described above in connection with Eq. 45 to enable the circuitry of Fig. 21 to perform an electronic function that varies with the C_V value.

[0223] Body voltage V_B in the circuitry of Fig. 21 can generally go as low as low supply voltage V_{LL} and as high as high supply voltage V_{HH}. The sum of gate-to-body voltage V_{GB} and body voltage V_B can often be as high as high supply voltage V_{HH}. Accordingly, gate-to-body voltage V_{GB} can often be varied across a range extending from zero to $V_{HH} - V_{LL}$. Inasmuch, as plate-to-body bias voltage V_R equals $V_{GB} - V_{VS} - V_Z$, minimum plate-to-body voltage V_{Rmin} is normally $-(V_{VS} + V_Z)$ while maximum plate-to-body voltage V_{Rmax} is normally $V_{HH} - V_{LL} - V_{VS} - V_Z$. The V_{Rmin}-to-V_{Rmax} range is the full supply voltage range $V_{HH} - V_{LL}$.

[0228] The electronic circuitry, primarily symmetrical circuit 280, in Fig. 22 has a pair of capacitance signals path for respectively receiving varactors C1 and C2 to enable the circuitry to perform an electronic function dependent on variable capacitances C_V. Analogous to the electronic circuitry of Fig. 18, one end of the C1 capacitance signal path in the circuitry of Fig. 22 consists of high-bias capacitance signal path line 236 that terminates at circuit 280. One end of the C2 capacitance signal path similarly consists of further high-bias capacitance signal path line 262 that also terminates at circuit 280.

[0229] Symmetrical circuit 280 is formed with symmetrical internal circuitry 280I, high-bias impedance components Z1 and Z2, a pair of largely identical impedance components Z3 and Z4, and an additional impedance component Z5. Analogous to what occurs in the circuitry of Fig. 18, impedance components Z1 and Z2 are respective parts of a pair of high-bias electrically conductive DC paths which extend through circuit 280 and through which high-bias DC paths 236 and 262 are respectively coupled to voltage setter 274.

[0230] Analogous to impedance component ZU in the circuitry of Fig. 21, impedance component Z3 is part of an electrically conductive DC path which extends through circuit 280 and through which electrical line 276 connected to C1 gate electrode 112 is electrically coupled to the V_{HH} high voltage supply. Impedance component ~~Z4~~ Z4 is similarly part of an electrically conductive DC path which extends through circuit 280 and through which an electrical line 282 connected to C2 gate electrode 112 is electrically coupled to the V_{HH} supply. Analogous to impedance ~~components~~ component ZH in the circuitry of Fig. 21, impedance component Z5 is part of a electrically conductive DC path which extends through circuit 280 and through which voltage setter 274 is electrically coupled to the V_{HH} supply. Accordingly, impedance components ~~Z1,~~ Z3, ~~Z2,~~ Z4, and Z5 are parts of a pair of longer electrically conductive DC paths through ~~path lines 238~~ which paths 236 and 262 are electrically coupled to the V_{HH} supply.

[0231] Internal symmetrical circuitry 280I of circuit 280 consists of electronic circuitry configured symmetrically with respect to impedance components Z1 - Z5. Internal circuitry 280I can interact with components Z1 - Z5 in various ways. For purpose of generality, Fig. 22 simply depicts circuitry 280I as being connected to components Z1 - Z5 by five respective electrical lines. Similar to what was stated above about the four lines shown as connecting internal circuitry 270I to impedance components ZH, ZL, ZT, and ZU in Fig. 21, the lines shown as connecting circuitry 280I to components Z1 - Z5 in Fig. 22 are intended to represent interactions

rather than specific electrical connections. The comments made above the constituency of impedance components ZH, ZT, and ZU and about the ZH, ZT, and ZU connection points of the electrical lines shown as extending from internal circuitry 270I to components ZH, ZT, and ZU in the circuitry of Fig. 21 apply here to components Z1 - Z5 and the electrical lines illustrated as connecting circuitry 280I to components Z1 - Z5 in the circuitry of Fig. 22.

[0232] Internal circuitry 280I is also connected to the V_{LL} low voltage supply. Circuitry 280I may be connected to the V_{LL} supply by multiple paths. As with earlier internal circuitry 260I, circuitry 280I may be connected to the V_{HH} high voltage supply by multiple paths separate from those going through impedance components Z1 - Z5. These supply-voltage paths are arranged symmetrically in circuit 280I. Consequently, circuitry 280I is internally symmetrical and is symmetrically configured relative to varactors C1 and C2. Examples of the symmetrical nature of circuitry 280I are presented below in connection with Figs. 23a and 23b.

[0233] Control system 272 in the circuitry of Fig. 22 is configured with respect to, and controls, varactor C1 in the same way as in the circuitry of Fig. 21. The same applies to varactor C2. Hence, voltage source 278 provides body voltage V_B on low-bias control line 242 to body electrodes 116 of varactors C1 and C2. Voltage source 278 is here connected to the V_{LL} low voltage supply by way of an electrical line 284.

[0234] Similar to the circuitry of Fig. 18, the second ends of the C1 and C2 capacitance signal paths terminate at the V_{LL} low voltage supply in the circuitry of Fig. 22. The C1 capacitance signal path in Fig. 22 specifically consists of high-bias capacitance signal path line 236, C1 plate electrode 114, C1 body electrode 116, control line 242, voltage source 278, and electrical line 284. The C2 capacitance signal path similarly consists of high-bias capacitance signal path line 262, C2 plate electrode 114, C2 body electrode 116, line 242, voltage source 278, and line 284. Gate electrodes 112 of varactors C1 and C2 are again outside the capacitance signal paths.

[0235] Also similar to what was said above about the circuitry of Fig. 18, varactors C1 and C2 in the circuitry of Fig. 22 can alternately be considered to be in a single capacitance signal path that bypasses voltage source 278. The single capacitance signal path then consists of high-bias path line 236, C1 plate electrode 114, C1 body electrode 116, control line 242, C2 body electrode 116, C2 plate electrode 114, and high-bias path line 262 just as in circuitry of Fig. 18. Gate electrodes 112 are outside the single capacitance signal path in the circuitry of Fig. 22.

[0241] Impedance components Z3 - Z5 are each of largely zero impedance in the VCO of Fig. 23a. In other words, components Z3 - Z5 are simply electrical lines in this VCO. Impedance voltage drop V_Z is therefore largely zero. Also, each of plate voltages V_G and V_{GP} is substantially high supply voltage V_{HH} in the VCO of Fig. 19a.

[0242] Voltage setter ~~272~~ 274 is implemented as a p-n diode D2 which couples the V_{HH} supply to the upper ends of inductors L1 and L2. Setter voltage drop V_{VS} here is a diode forward voltage drop V_F of 0.5 - 0.9 V, again typically 0.7 V. Diode D2 and current source I1 cooperate to set the specific value of diode drop V_F. As with diode D1 and current source I1 in the VCO of Fig. 19, increasing the size of current source I1 so as to increase its current causes voltage V_F to increase, and vice versa. Since impedance voltage V_Z is largely zero, each of DC gate-to-plate bias voltage V_{GP} and V_{GPF} is largely setter voltage drop V_{VS} and thus equals V_F. Each of DC plate voltages V_P and V_{PF} is largely fixed at $V_{HH} - V_F$.

[0243] The VCO of Fig. 23a operates in the following manner. When high supply voltage V_{HH} is raised to a sufficiently high value above low supply voltage V_{LL}, the VCO begins to oscillate. Plate-to-body bias voltages V_R and V_{RF} are controlled in the manner described above in connection with the general circuitry of Fig. 22. Accordingly, the VCO of Fig. 23a provides an oscillator signal (not specifically indicated) from the drain of FET Q1 or Q2 at oscillator frequency f_O given by Eq. 42.

[0244] Body voltage V_B can be varied from low supply voltage V_{LL} almost all the way up to high supply voltage V_{HH}, i.e., to within amount V_Y of voltage V_{HH}, in the VCO of Fig. 22. Amount V_Y here is typically 0.1 V but can be higher or lower, e.g., substantially all the way down to zero. End-range values V_{Rmax} and V_{Rmin} of gate-to-body voltage V_R or V_{RF} respectively are $V_Y - V_F$ and $V_{HH} - V_{LL} - V_F$ where V_F again is 0.6 - 0.7 V, typically 0.7 V.

[0245] Fig. 23b depicts another VCO implementation of the circuitry of Fig. 22. Except as described below, the VCO of Fig. 23 contains varactors C1 and C2, FETs Q1 and Q2, inductors L1 and L2, and current source I1 configured and operable the same as in the VCO of Fig. 23a. Hence, internal circuitry 280I again consists of FETs Q1 and Q2 and current source I1, while impedance components Z1 and Z2 are implemented with inductors L1 and L2.

[0246] In place of diode D2, voltage setter 274 is implemented with a level-shifting p-channel enhancement-mode insulated-gate FET Q3 in the VCO of Fig. 23b. The source of FET Q3 is

value that can be achieved for area A_P with that set of design rules. This facilitates achieving a high A_I/A_P area ratio and thus a high C_{Vmax}/C_{Vmin} varactor capacitance ratio.

[0257] A layer 290 of dielectric material overlies field insulating region 134 and semiconductor islands 136 and 138 above gate electrode 112 in the varactor of Figs. 24 and 25. Plate electrode 114 contacts plate region 102 through a plate contact opening 292 extending through dielectric layer 290. Body electrode 116 contacts body contact portion 132 of body region 100 through a group, ~~14~~ fourteen in the exemplary layout of Fig. 24, of body contact openings 294 extending through layer 290. Body contact openings 294 are distributed relatively uniformly across the lateral area occupied by body contact portion 132 to provide uniform electrical connection to body region 100. A gate contact opening 296 extends through layer 290. An electrical conductive gate line 298, typically consisting of the same metallic material as plate electrode 114 and body electrode 116, contacts gate electrode 112 through gate contact opening 296.

[0258] Fig. 26 depicts a layout, in accordance with the invention of another preferred implementation of the n-channel varactor of Fig. 8. The layout of Fig. 26 is directed toward improving the varactor's quality factor. Fig. 27 illustrates a cross section of the n-channel varactor of Fig. 26 taken along a vertical plane extending through plate region 102. Except as indicated below, the varactor of Figs. 26 and 27 is arranged the same as the varactor of Figs. 24 and 25.

[0259] In the varactor of Figs. 26 and 27, plate region 102 consists of a main plate portion 102M and one or more, normally at least two, finger portions 102F which are continuous with, and extend laterally away from, main plate portion 102M. As viewed generally perpendicular to upper semiconductor surface 106, main plate portion 102M is roughly square shaped in the exemplary layout of Fig. 26. Nonetheless, plate portion 102M can have other lateral shapes. For example, plate portion 102M can be rectangular, octagonal, hexagonal, circular, and so on as viewed perpendicular to upper surface 106.

[0260] Each finger portion 102F extends into semiconductor material that would otherwise form part of body region 100 in semiconductor island 136. Accordingly, each finger portion 102F meets body region 100 to form part of p-n junction 104. When there are two or more finger portions 102F in the varactor, portions 102F are distributed laterally around main plate portion